

**FIG. 1** basic power delivery system

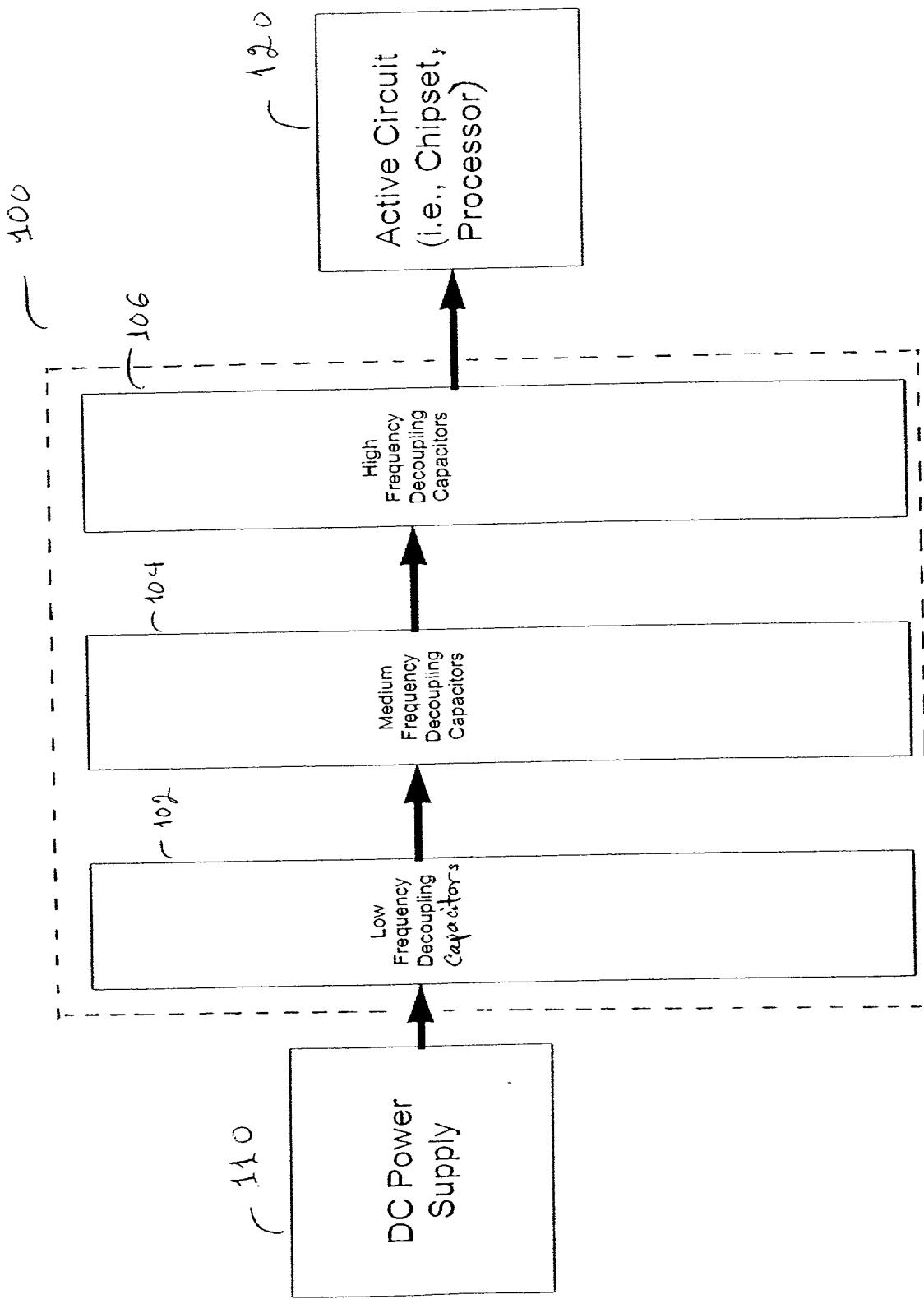


FIG. 2

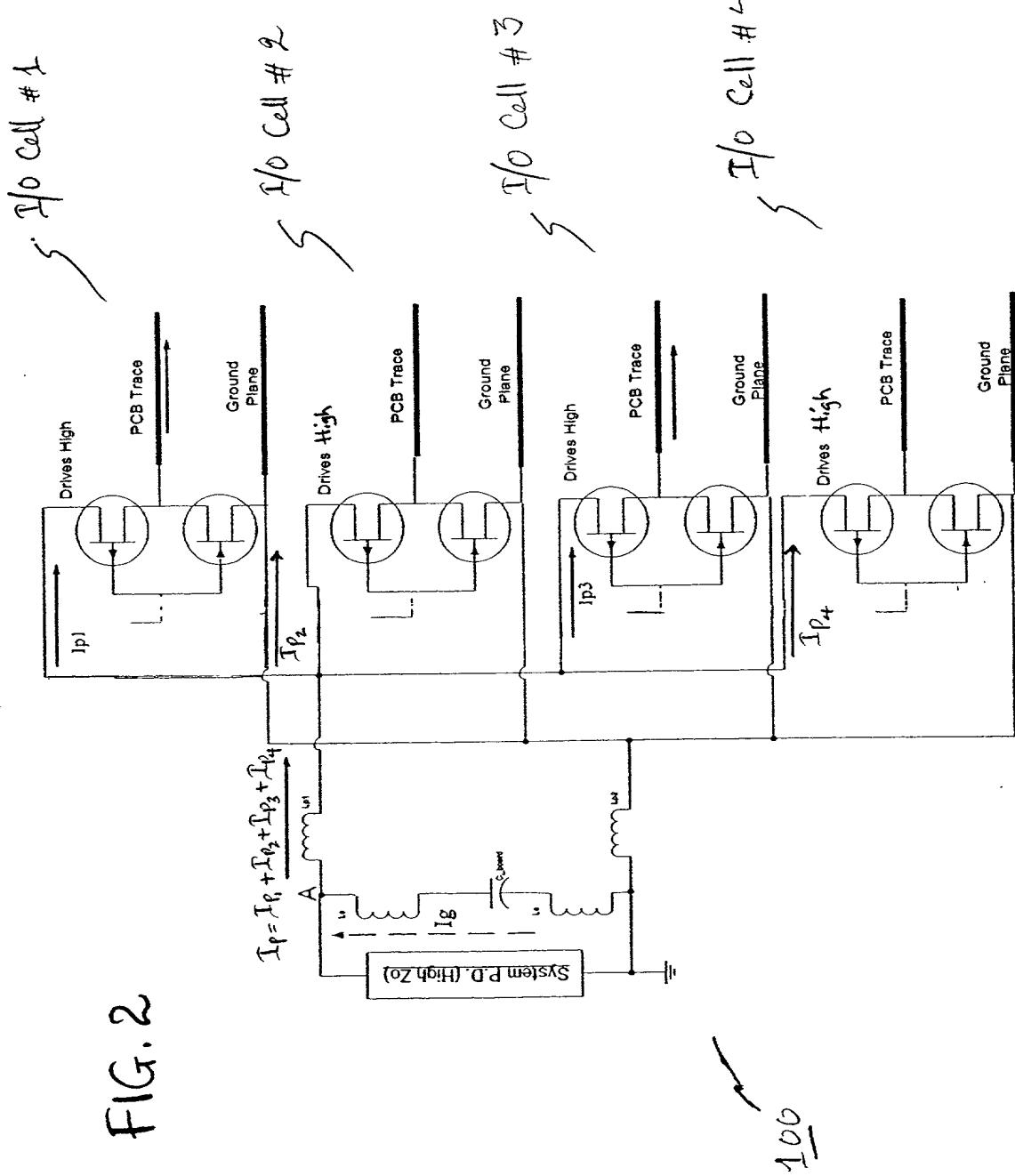


Figure 3 shows a circuit diagram for a memory array with four cells. The circuit includes a Pre-Driver, Low Weight Encoding Circuity, and a System P.D. (High Z<sub>o</sub>) output.

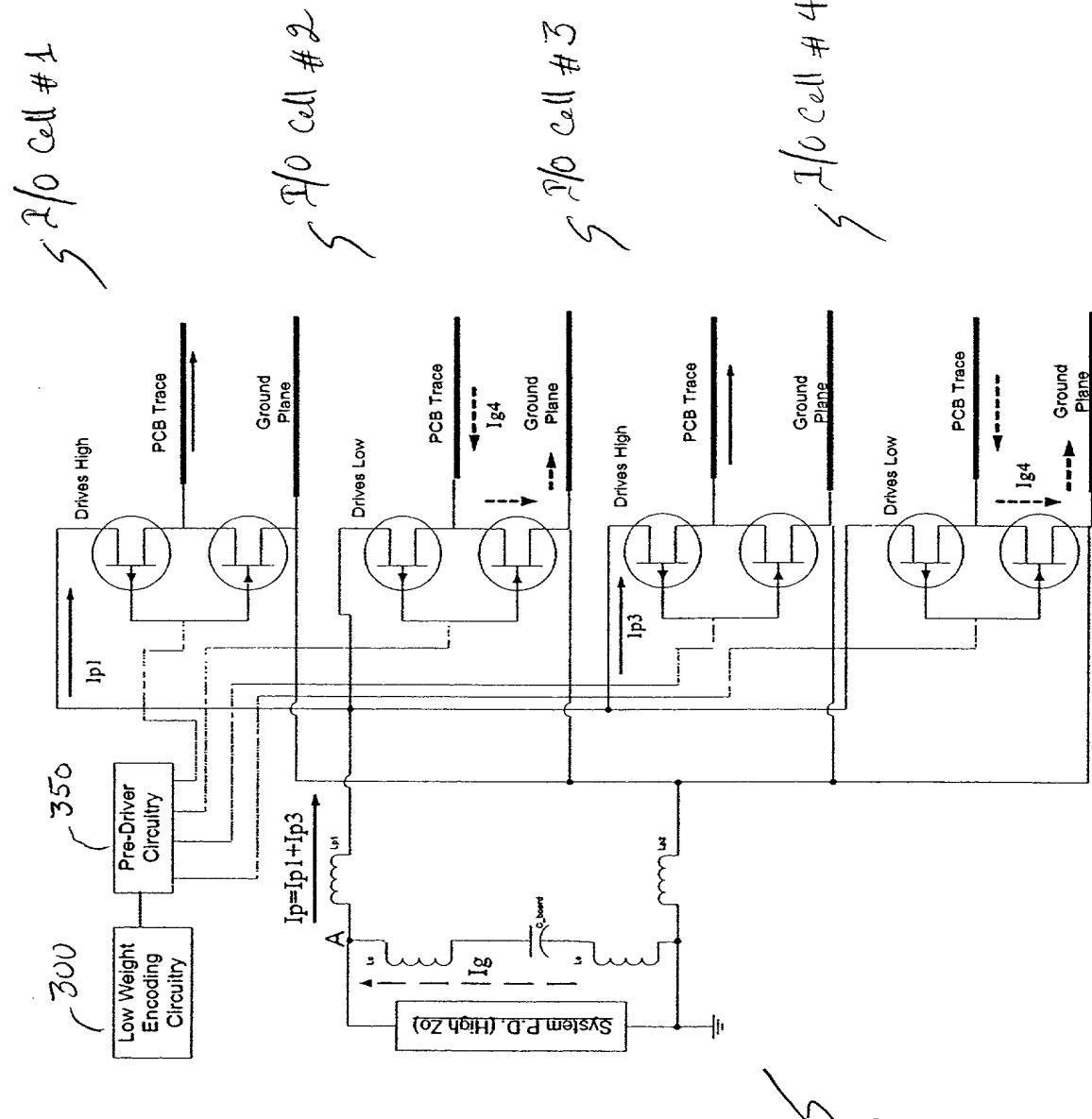


FIG. 3

100

FIG. 4

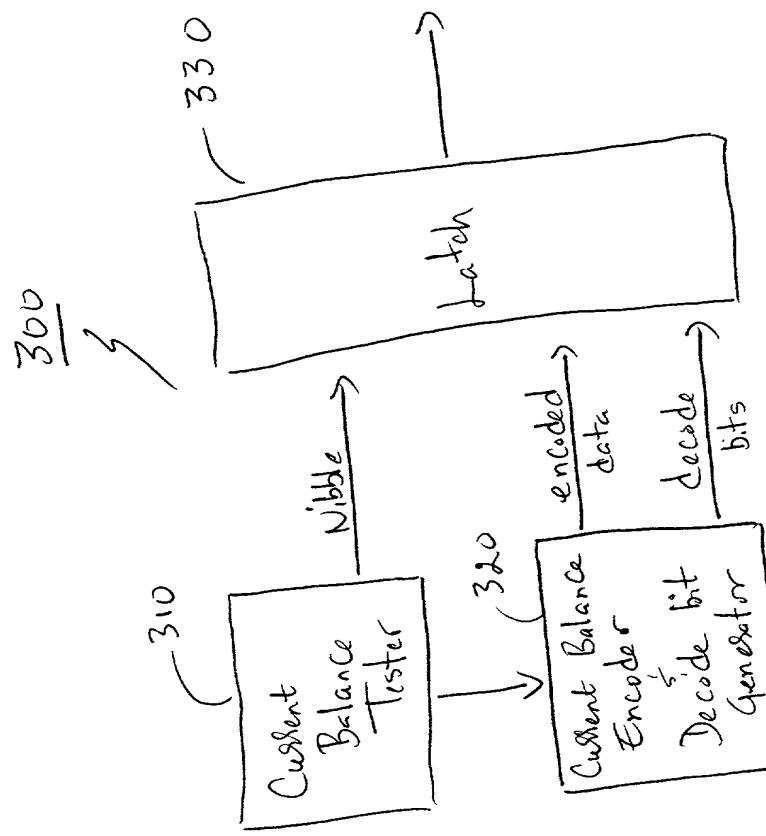


FIG. 5

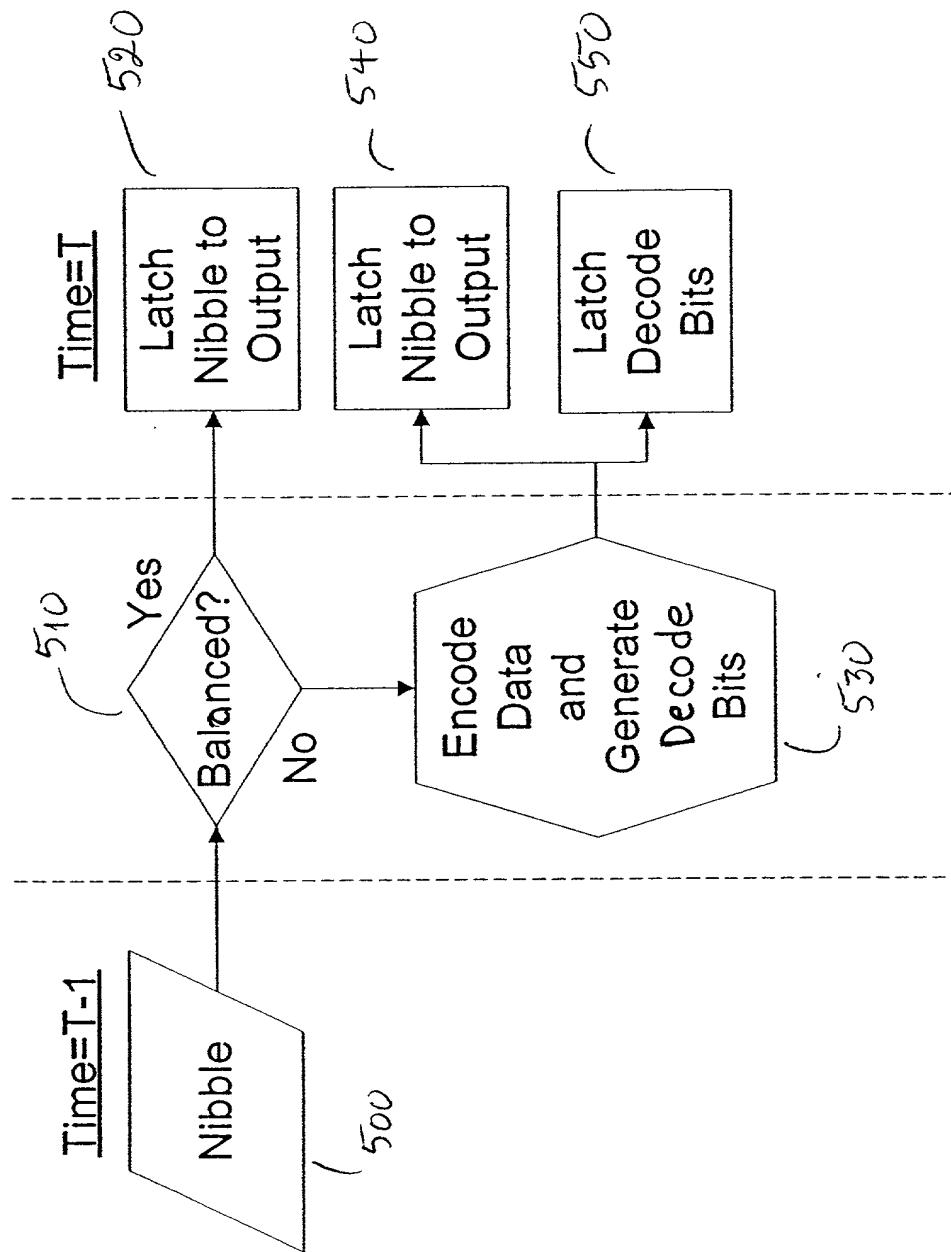


FIG. 6 A

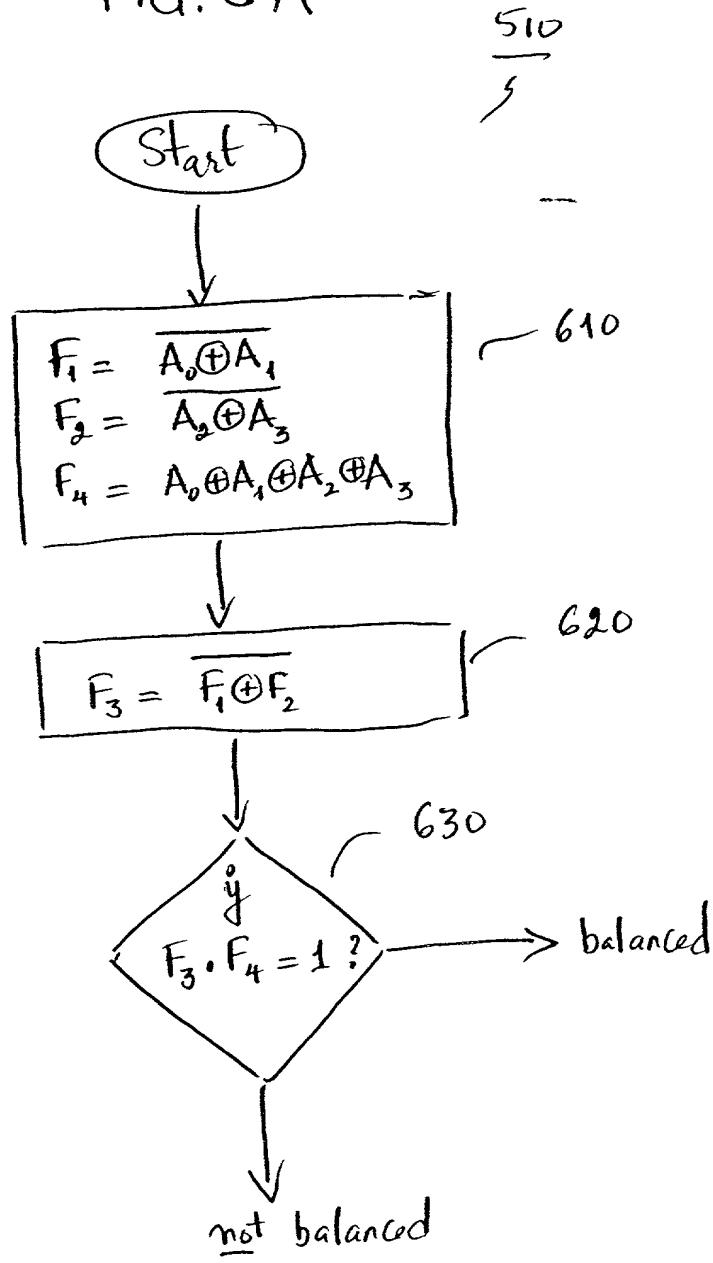


FIG. 7A

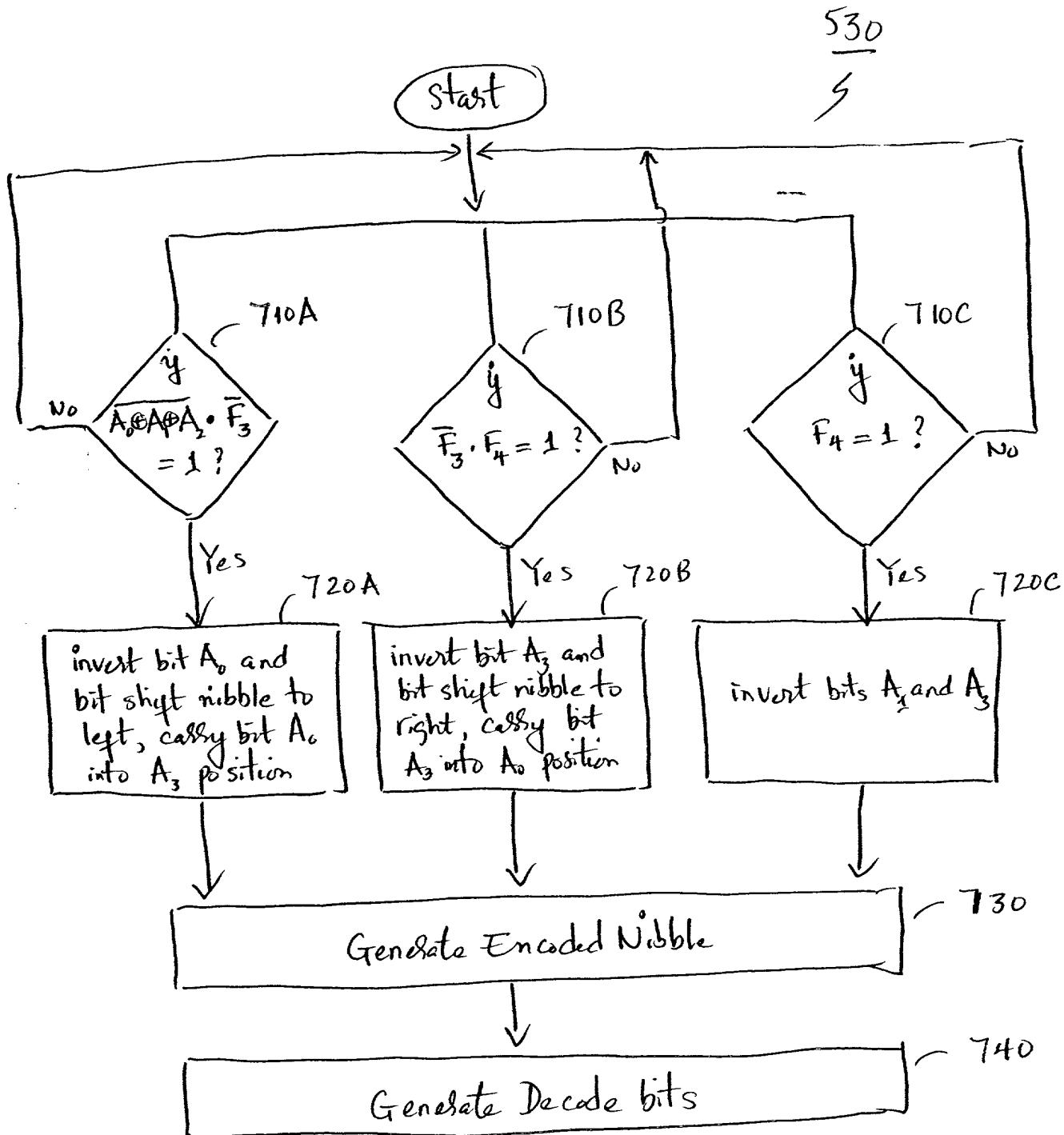


FIG. 6B - TABLE #1

$A_0$	$A_1$	$A_2$	$A_3$	$F_1$	$F_2$	$F_3$	$F_4$	$F_3 \bullet F_4$
0	0	0	0	1	1	1	0	0
0	0	0	1	1	0	0	1	0
0	0	1	0	1	0	0	1	0
0	0	1	1	1	1	1	1	1
0	1	0	0	0	1	0	1	0
0	1	0	1	1	0	0	1	1
0	1	1	0	0	0	0	1	1
0	1	1	1	1	0	0	1	1
1	0	0	0	1	0	1	0	0
1	0	0	1	0	0	0	1	0
1	0	1	0	0	1	0	1	0
1	0	1	1	1	0	1	1	1
1	1	0	0	1	1	0	0	0
1	1	0	1	0	1	0	1	0
1	1	1	0	1	1	0	1	0
1	1	1	1	1	1	1	1	1

FIG. 7B - TABLE #2

$\underline{A0}$	$\underline{A1}$	$\underline{A2}$	$\underline{A3}$	Right Shift	Left Shift	Invert	$\underline{A0}$	$\underline{A1}$	$\underline{A2}$	$\underline{A3}$	Decode Bits
0	0	0	0	x	x	x	0	1	0	1	1
0	0	0	1	x	x	x	0	0	1	1	0
0	0	1	0	x	x	x	1	0	0	0	1
0	0	1	1	x	x	x	1	0	1	0	1
0	1	0	0	x	x	x	0	0	1	1	0
1	0	0	1	x	x	x	1	1	0	0	1
1	0	1	0	x	x	x	0	1	0	0	1
1	1	0	1	x	x	x	0	1	1	0	1
1	1	1	0	x	x	x	1	1	0	0	0
1	1	1	1	1	1	1	1	0	1	0	1